

Fig. 1

09516408.021400

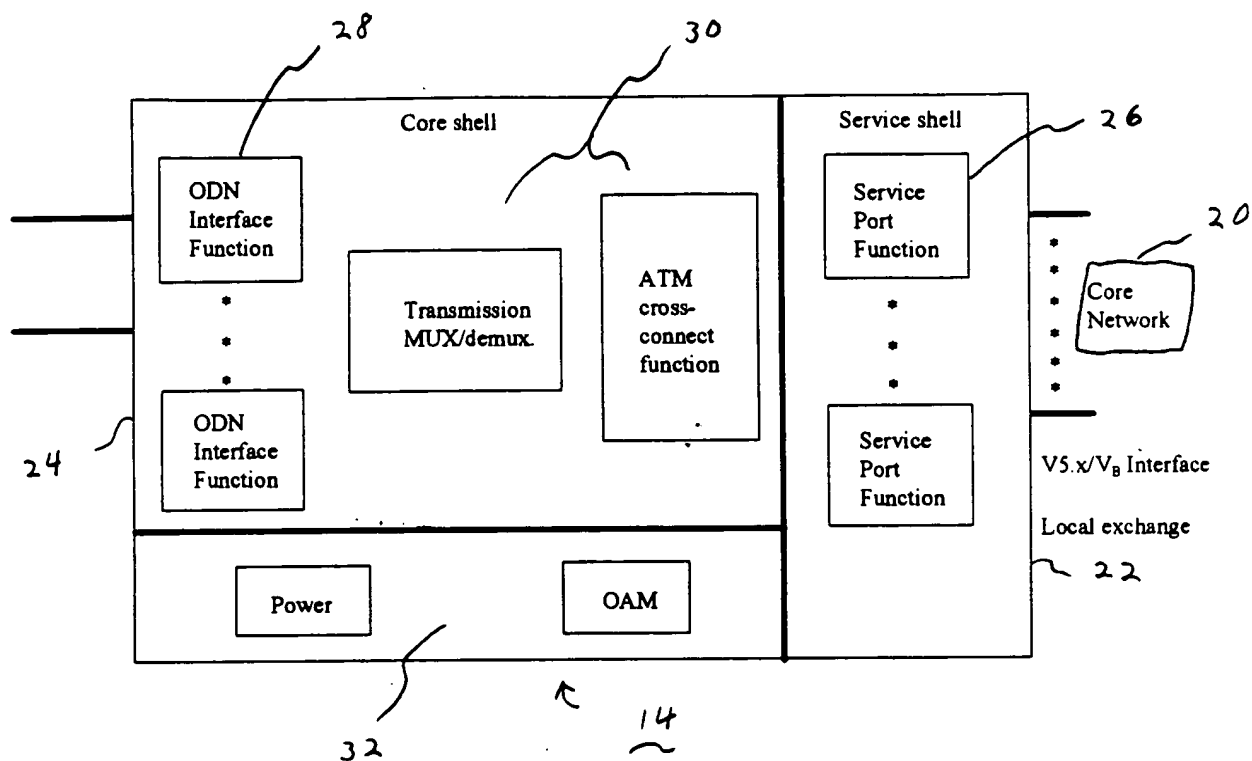
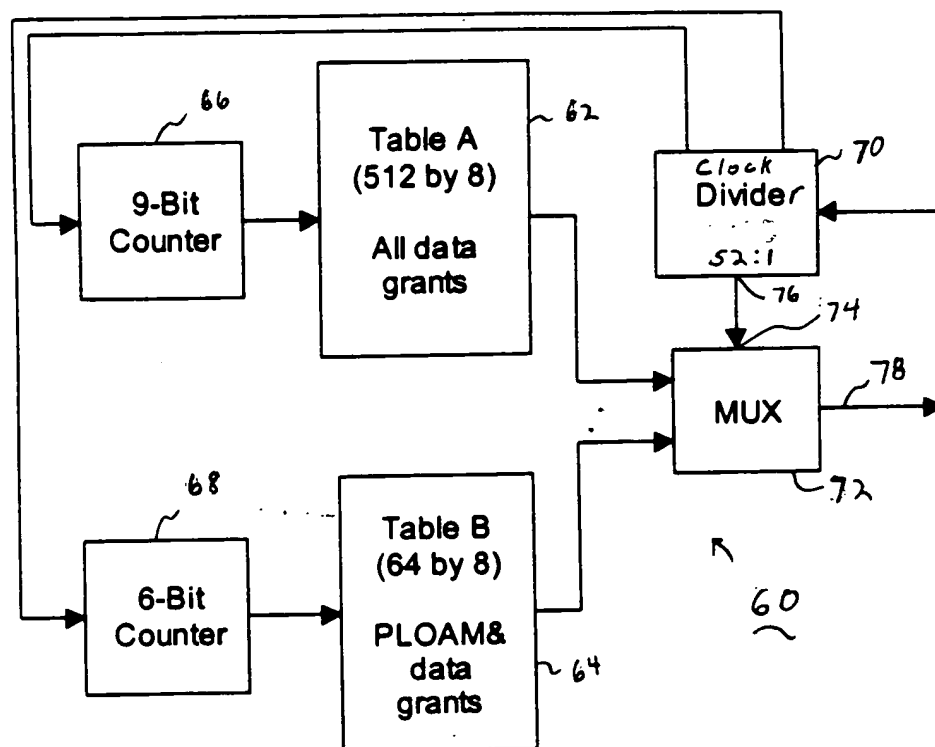
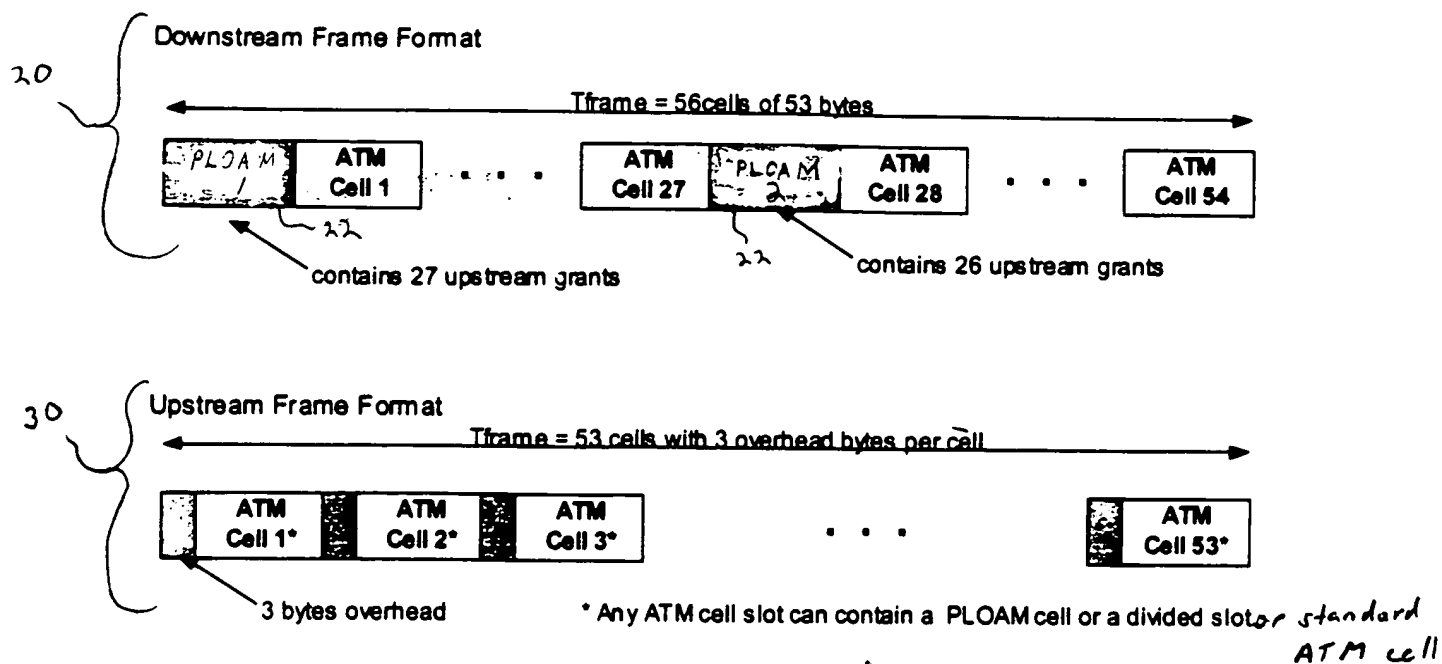


Fig. 2

090316Z 071000



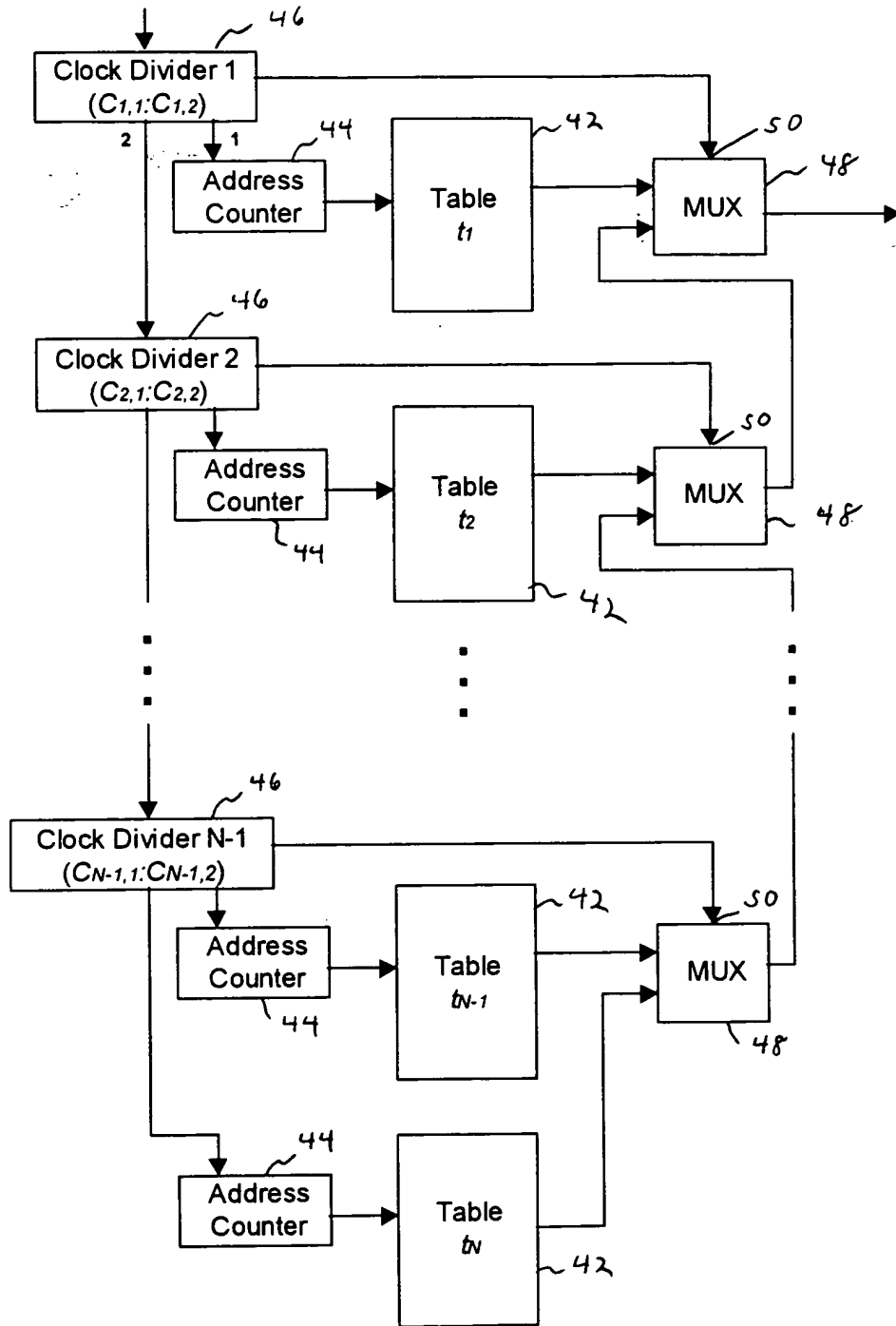


Figure 4. Recursive implementation of grant generator using multi-tables.

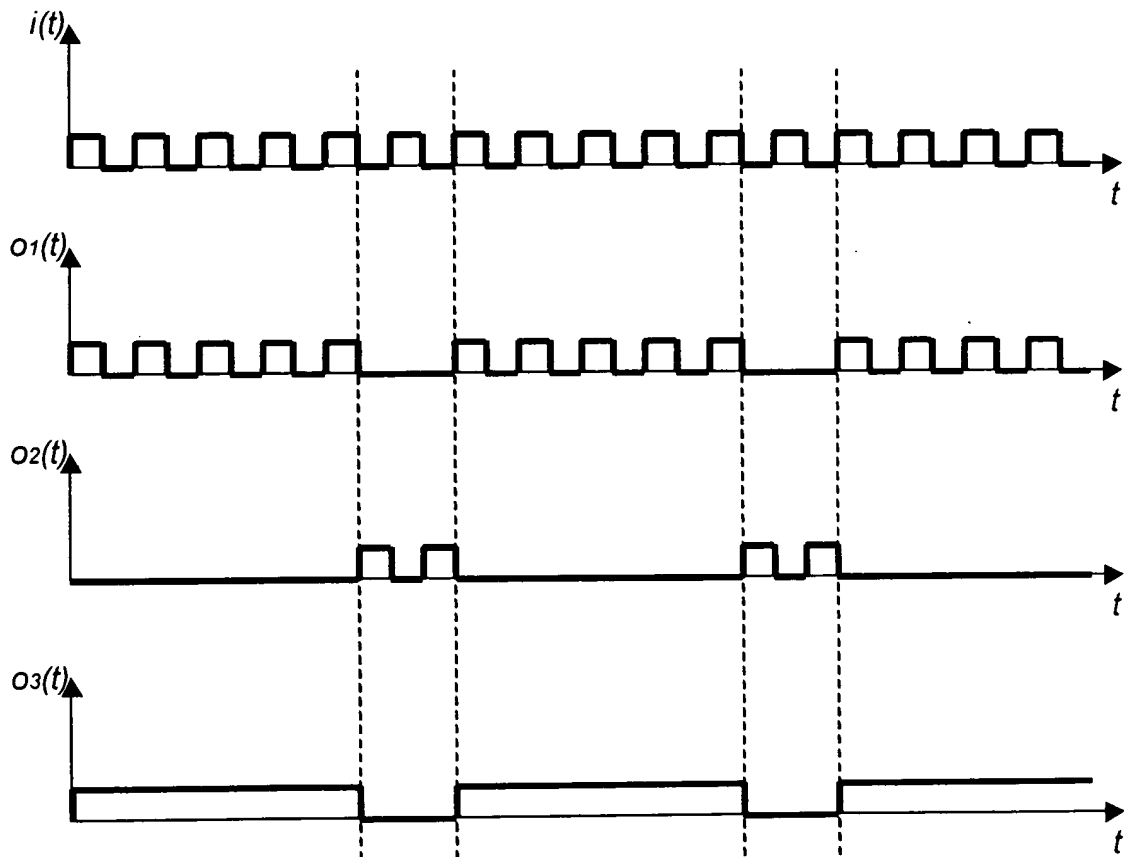
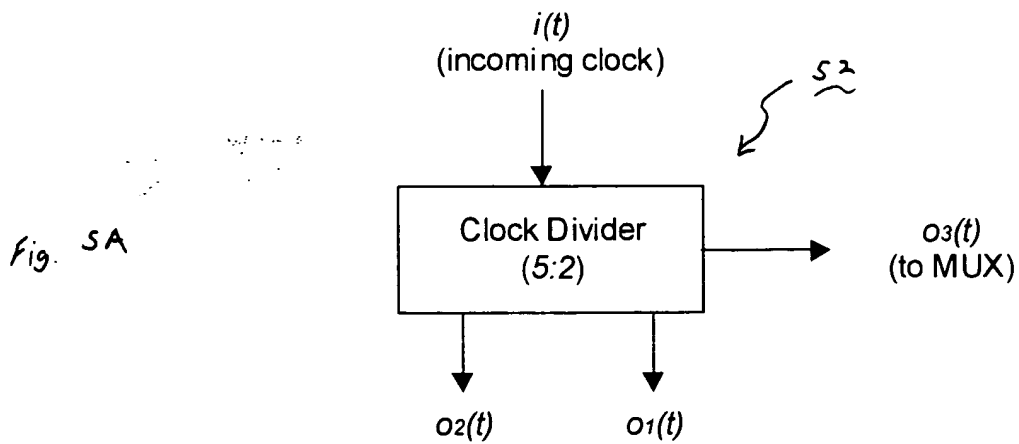


Figure 5B Example timing diagram for input and output signals of clock divider with division ratio 5:2.

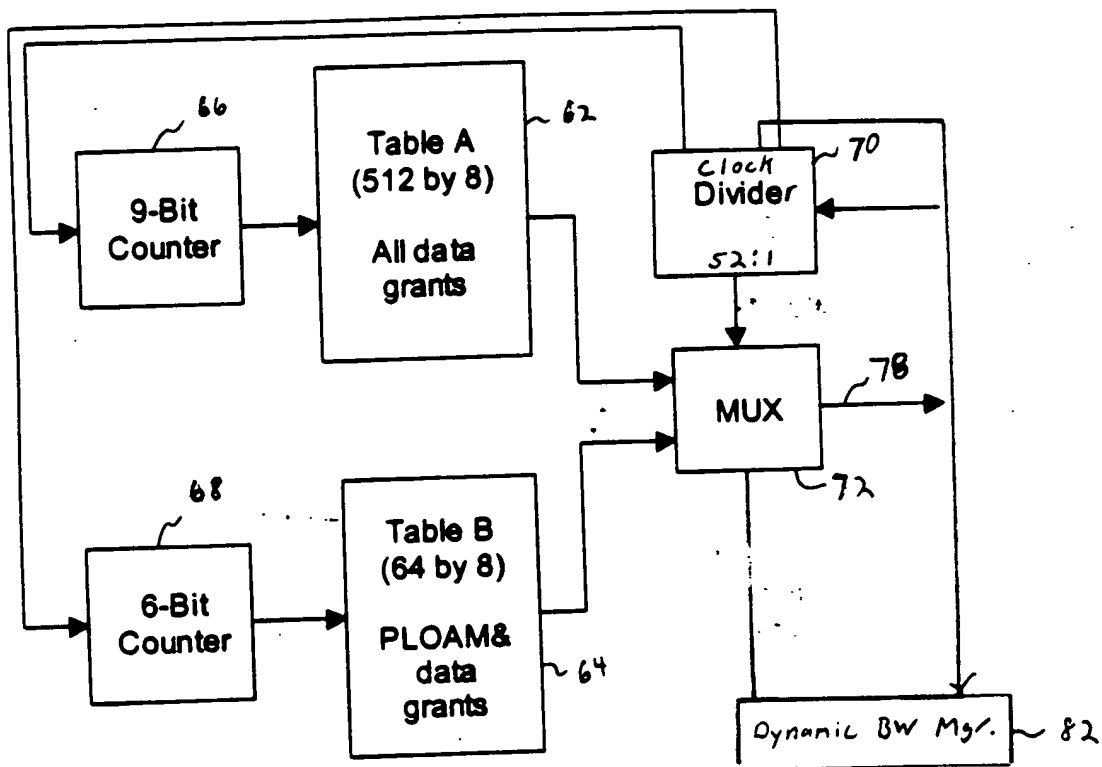


Fig 7